

**DIONICS INC.**

65 RUSHMORE ST., WESTBURY, N.Y. 11590 516-997-7474



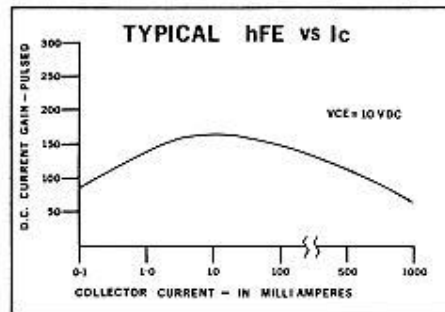
2N2907A·2N2905A  
2N2906A·2N2904A

2N2907·2N2905  
2N2906·2N2904

PNP SILICON

HIGH CURRENT (1.0 AMP) TRANSISTOR CHIPS  
DESIGNED FOR HYBRID CIRCUIT APPLICATIONS.

The high efficiency parallel emitter construction provides improved beta retention at high current levels. The large area bonding pads are positioned for maximum flexibility of substrate layout. Unique surface stabilization processing results in lower leakage currents and prevents the beta degradation frequently encountered during the extended high temperature assembly operations required for complex hybrid circuit construction. Chips are gold backed for eutectic die-attach, and have aluminum bonding pads for all conventional wire bonding techniques.



← 100% Probe Tested to These Parameters @ 25°C → ← Guaranteed →  
(tested on sample basis)

	h <sub>FE</sub> @ V <sub>CE</sub> =10V			V <sub>CE0</sub> Volts Min. @ I <sub>C</sub> = 10 $\mu$ A I <sub>E</sub> =0	V <sub>CE5</sub> Volts Min. @ I <sub>C</sub> = 10mA I <sub>E</sub> =0	V <sub>FE0</sub> Volts Min. @ I <sub>E</sub> = 10 $\mu$ A I <sub>C</sub> =0	I <sub>FE0</sub> nA Max. @ V <sub>CE</sub> = 50V I <sub>E</sub> =0	V <sub>CE</sub> (SAT.) Volts Max. @ I <sub>C</sub> =150mA I <sub>E</sub> =15mA	C <sub>02</sub> pF Max. @ V <sub>CE</sub> =10V f <sub>i</sub> =0 f=100KHz	f <sub>T</sub> MHz Min. @ I <sub>C</sub> =50mA V <sub>CE</sub> =20V f=100MHz
	@ I <sub>C</sub> = 1mA	@ I <sub>C</sub> = 10mA	@ I <sub>C</sub> = 150mA							
2N 2907A 2N 2905A	100 MIN	100 MIN	100- 300	60	60	5	10	0.4	8	200
2N 2906A 2N 2904A	40 MIN	40 MIN	40- 120							
2N 2907 2N 2905	50 MIN	75 MIN	100- 300	60	40	5	20	0.4	8	200
2N 2906 2N 2904	25 MIN	35 MIN	40- 120							

Dimensional Drawing on Reverse Side

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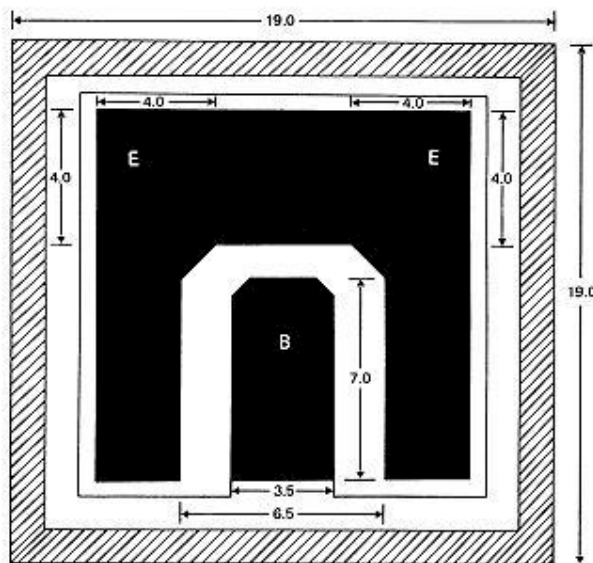


2N2907·2N2905

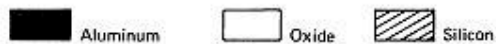
2N2906·2N2904

PNP SILICON

HIGH CURRENT (1.0 AMP) TRANSISTOR CHIPS  
DESIGNED FOR HYBRID CIRCUIT APPLICATIONS.



Dimensions in Mils



- Chip Thickness=6 Mils  $\pm$ 1 Mil
- Min. Dimension Across Bonding Pads=3.5 Mils
- Min. Separation Between Bonding Pads=1.0 Mils
- Distance from Bonding Pads to Edge of Chips=2.5 Mils

Detailed Specifications on Reverse Side