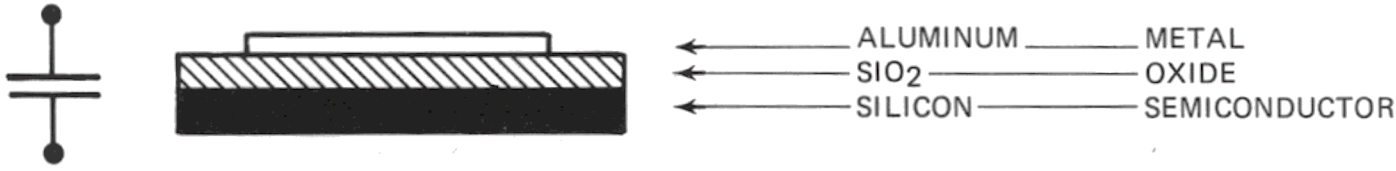
DIONICS INC.
65 Rushmore Street, Westbury, N.Y. 11590 (516) 997-7474

VARIABLE-FIXED CAPACITORS

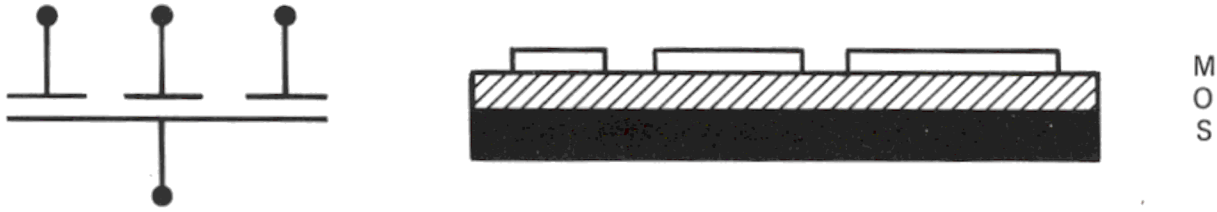
By George Seaton

A novel chip component for use in hybrid circuits has made the scene and is finding great utility in crystal controlled oscillators, such as those found in digital wristwatches. The component is a multiple valued MOS capacitor chip which is used for trimming oscillator frequency. MOS capacitors are produced by conventional semiconductor manufacturing techniques. A controlled layer of oxide (SIO_2) is thermally grown on a silicon substrate, and aluminum bonding pads are vacuum deposited on the top surface of the oxide. The silicon substrate serves as one plate of the capacitor, the oxide is the dielectric, while the aluminum bonding pad serves as the opposing plate.



The capacitance value is determined by the thickness of the oxide and the surface area dimensions of the aluminum bonding pad.

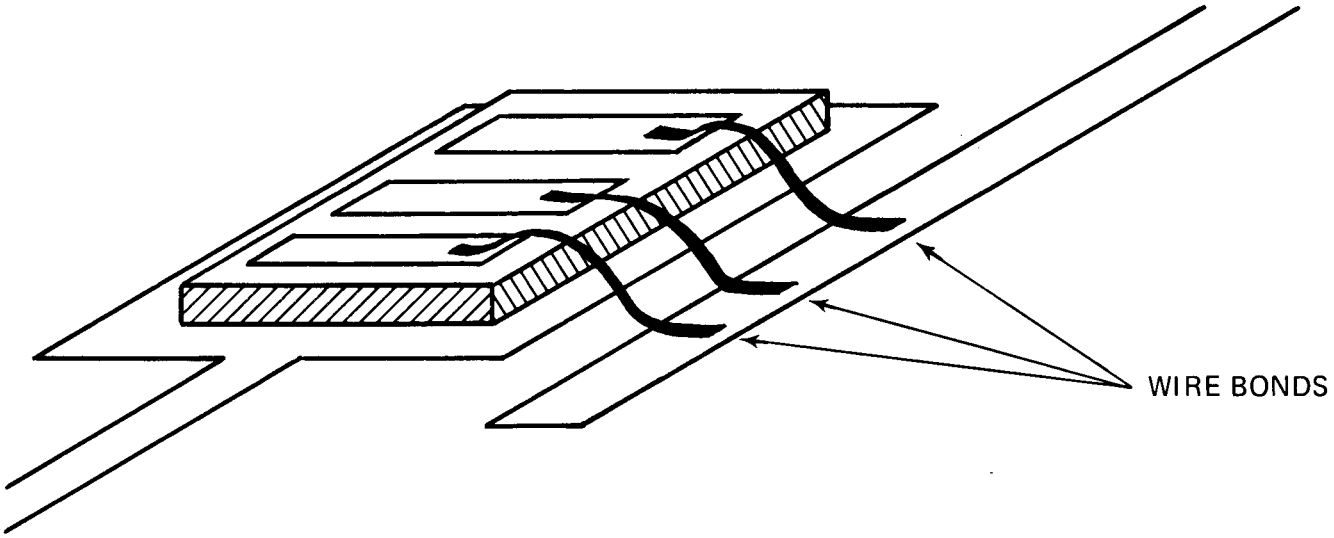
By building a chip which contains several separate aluminum pads of differing dimensions, a multiple capacitor is formed which uses the silicon substrate as a common plate.



In application, the chip is die bonded to a conductive path on the hybrid substrate. All aluminum pads are wire bonded to a second conductive path (see diagram on reverse side) which places all of the separate capacitors in parallel, forming a single capacitor whose value equals the sum of the individual values.

Forming part of the tuned circuit, this capacitor causes oscillation to begin at a specific frequency which can be conveniently monitored on a frequency counter or scope. Depending upon how far off this initial oscillation is from the desired frequency, the capacitor can now be trimmed by selectively breaking wire bonds to the aluminum pads which removes controlled segments of capacitance from the circuit. An operator can easily become proficient at selecting the proper values to remove in order to accomplish a given frequency change.

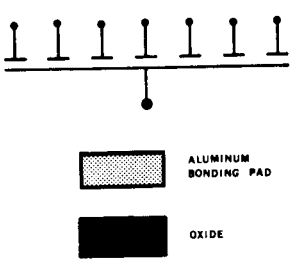
(continued on reverse side)



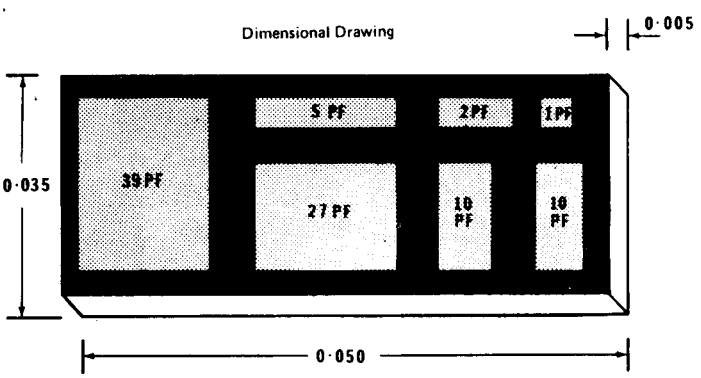
Total values of up to 200 PF per chip are considered reasonable while resolution of 0.5 PF can be achieved. Advantages offered by the chips are their small physical size (typically only 5 mils thick) the compatability of attachment by conventional chip & wire techniques and approximate NPO temperature coefficient characteristics. Two such chips, presently being used in crystal controlled watches are shown below.

The C-700 has a maximum total value of 94PF while the C-1248 totals 15 PF. Being a binary device, the C-1248 can be trimmed to any value from 1.0 PF to 15 PF in 1.0 PF increments.

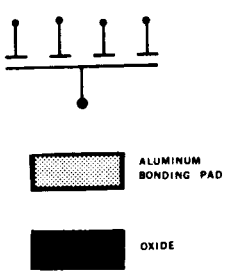
C - 700



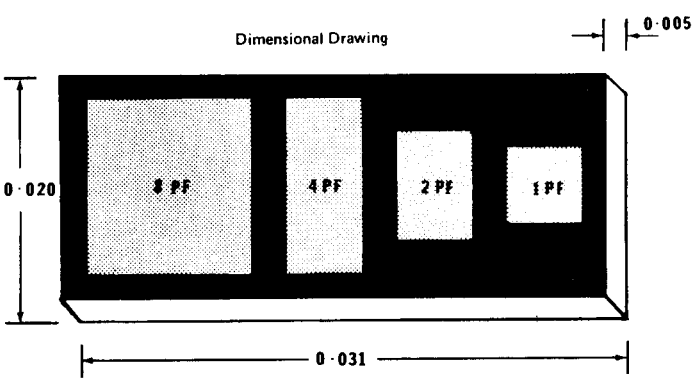
Dimensional Drawing



C - 1248



Dimensional Drawing



Each chip is gold backed and may be eutectically bonded with the chip bottom serving as one plate contact. An aluminum pad on the top of the chip surface is then contacted, using conventional wire bonding techniques.

MAXIMUM WORKING VOLTAGE	PROBED VOLTAGE
50V	100V

Tolerance = ±10% with 2% within a lot
Temperature Coefficient = +35 PPM ±15 PPM/°C
Dissipation Factor = 0.0001 to 0.00025 from -20°C to +150°C
Maximum Operating Temperature — +200°C

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